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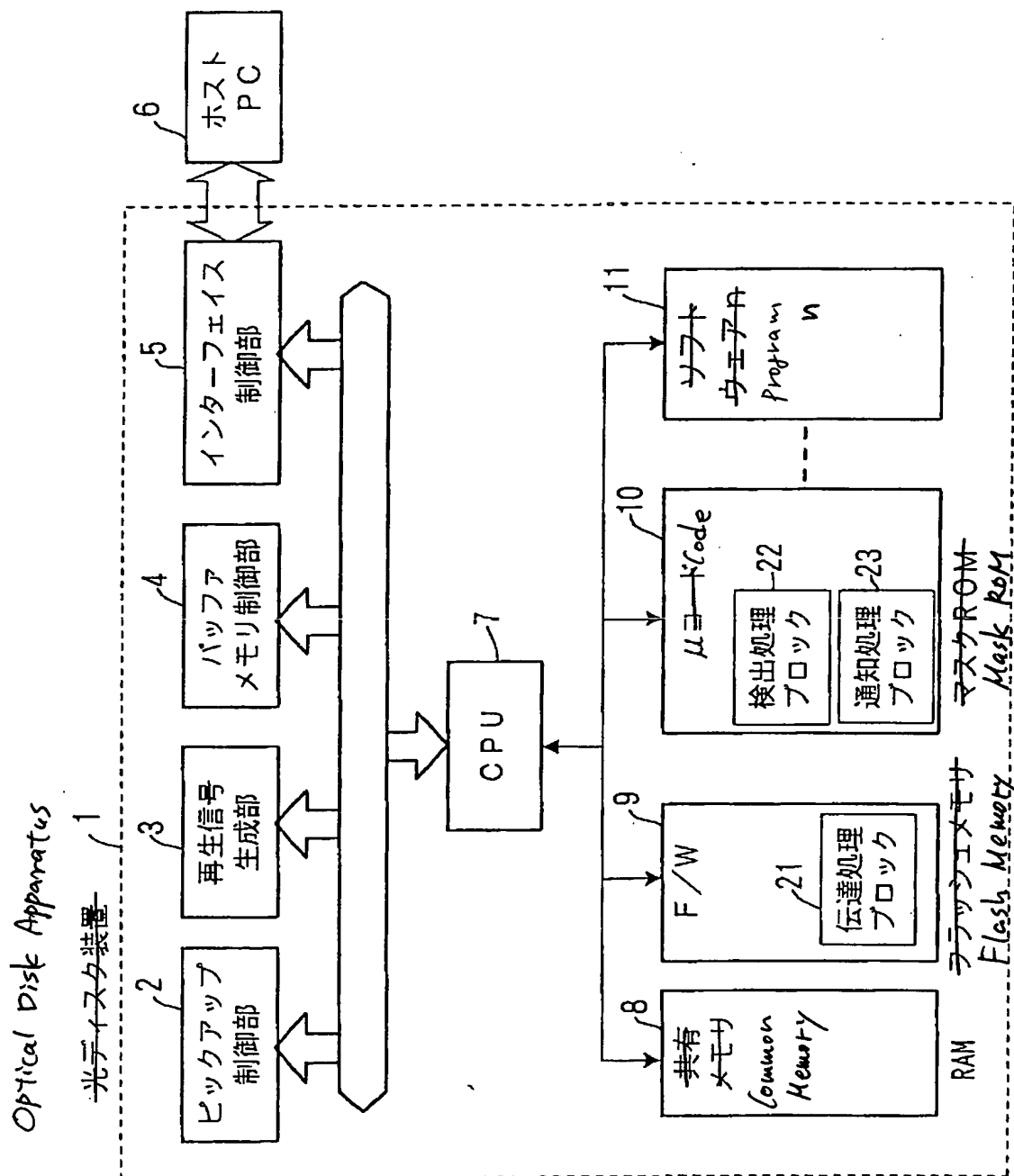
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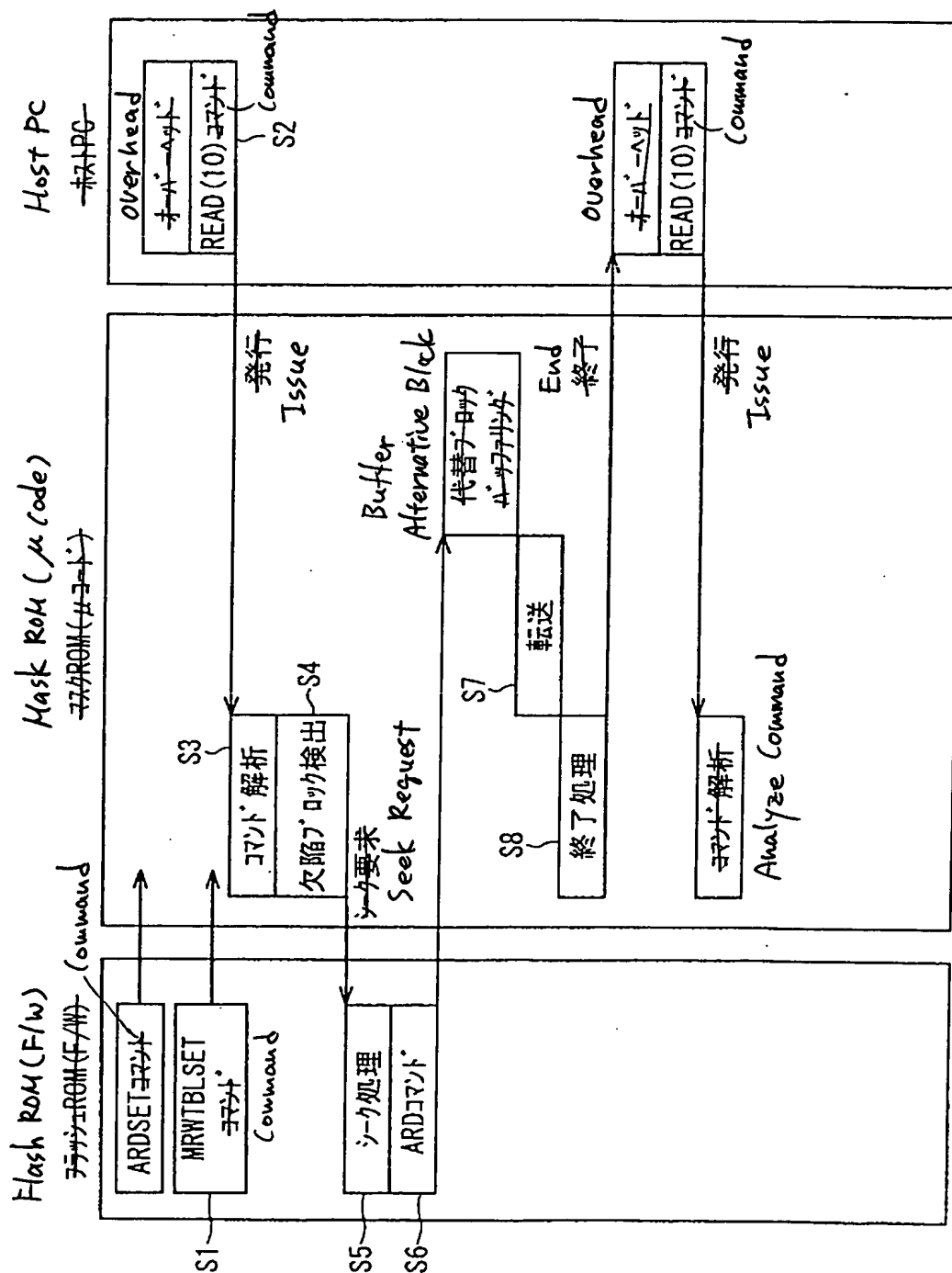
【書類名】 図面

【図1】 FIG. 1



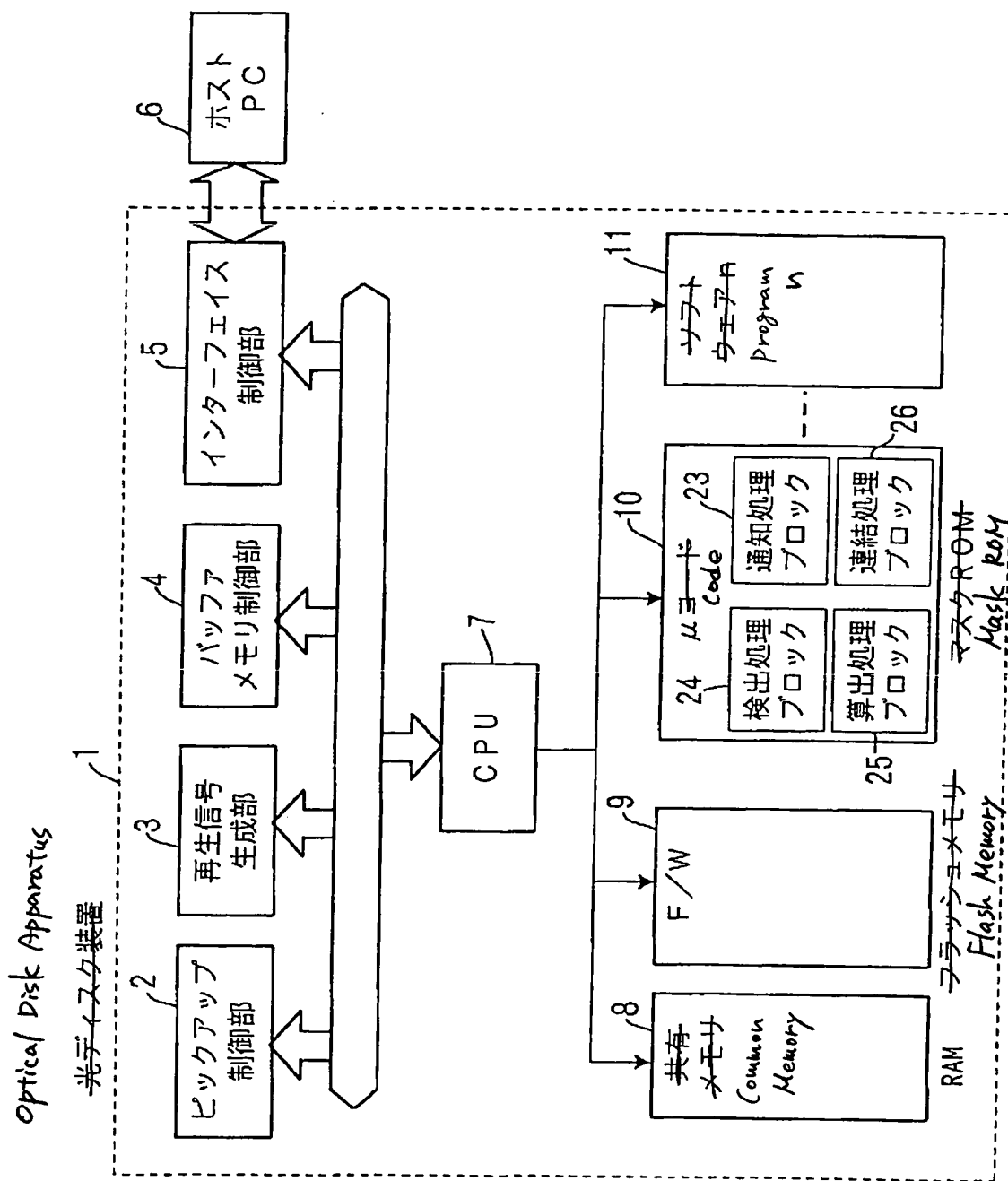
- 2: PICK-UP CONTROL SECTION
- 3: REPRODUCTION SIGNAL GENERATING SECTION
- 4: BUFFER MEMORY CONTROL SECTION
- 5: INTERFACE CONTROL SECTION
- 6: HOST PC
- 21: TRANSMISSION PROCESS BLOCK
- 22: DETECTION PROCESS BLOCK
- 23: NOTIFICATION PROCESS BLOCK

FIG. 2



- S3: ANALYZE COMMAND
- S4: DETECT DEFECTIVE BLOCK
- S5: SEEK PROCESS
- S6: ARD COMMAND
- S7: TRANSFER
- S8: TERMINATING PROCESS

図3 Fig.3



- 2: PICK-UP CONTROL SECTION
3: REPRODUCTION SIGNAL GENERATING SECTION
4: BUFFER MEMORY CONTROL SECTION
5: INTERFACE CONTROL SECTION
6: HOST PC
23: NOTIFICATION PROCESS BLOCK
24: DETECTION PROCESS BLOCK
25: CALCULATION PROCESS BLOCK
26: CONNECTING PROCESS BLOCK

~~【图5】~~ Fig. 5

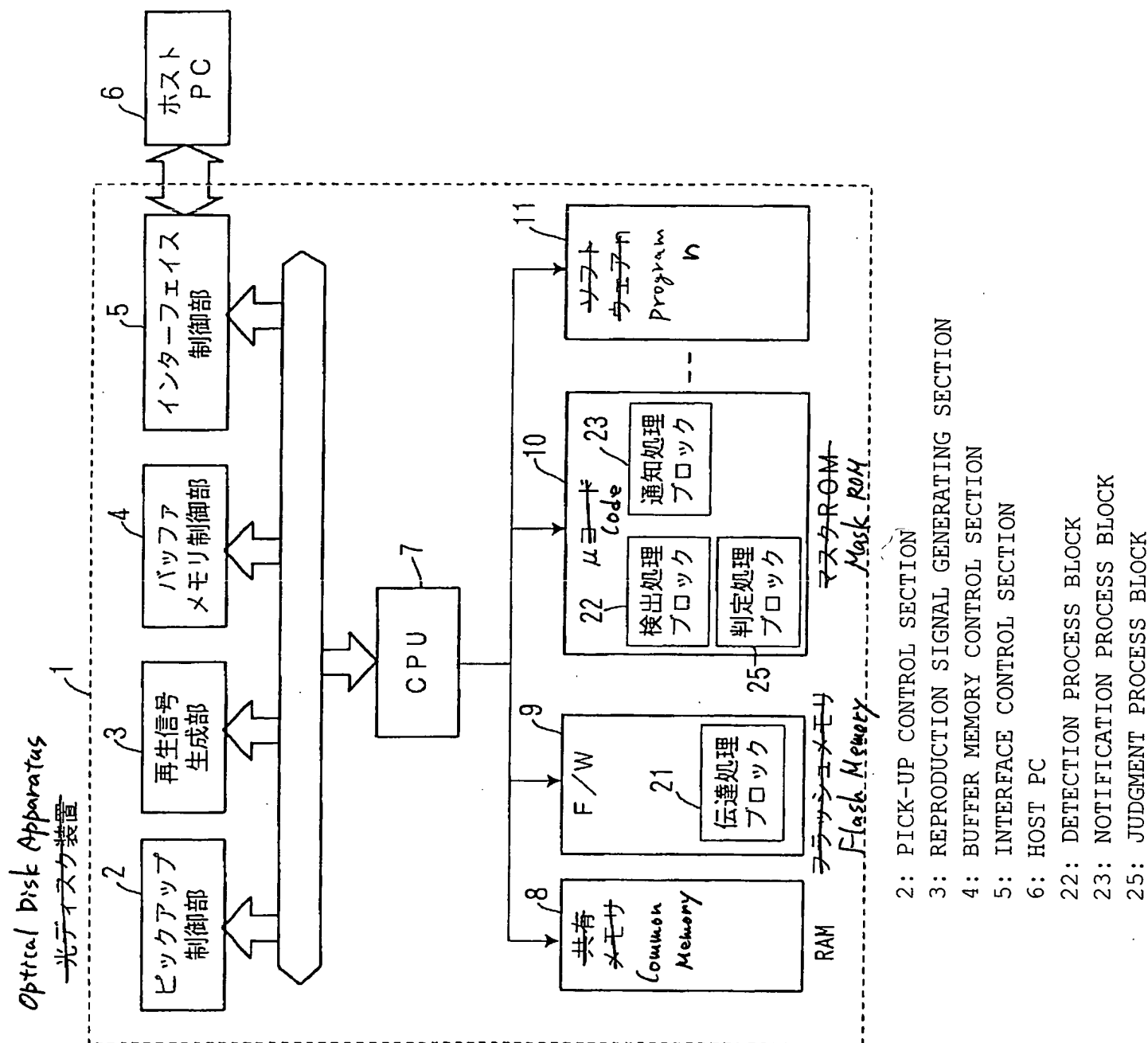


Figure 1 is a sequence diagram illustrating the control sequence of a disk control system. The diagram is divided into three main sections: Command, Data Transfer, and End.

Command Section:

- The host (left) sends commands: ARDSET (S31), MRWTBLSET (S31), and ARDPOINT (S36).
- The disk controller (right) receives these commands and processes them (S35).
- The disk controller issues a command (S32) to the host, which includes an Overhead and a READ(10) command.

Data Transfer Section:

- The disk controller performs command analysis (S33) and seeks (S34).
- The disk controller issues a command (S37) to the host, which includes an Overhead and a READ(10) command.
- The disk controller performs data transfer (S38) and final processing (S39).

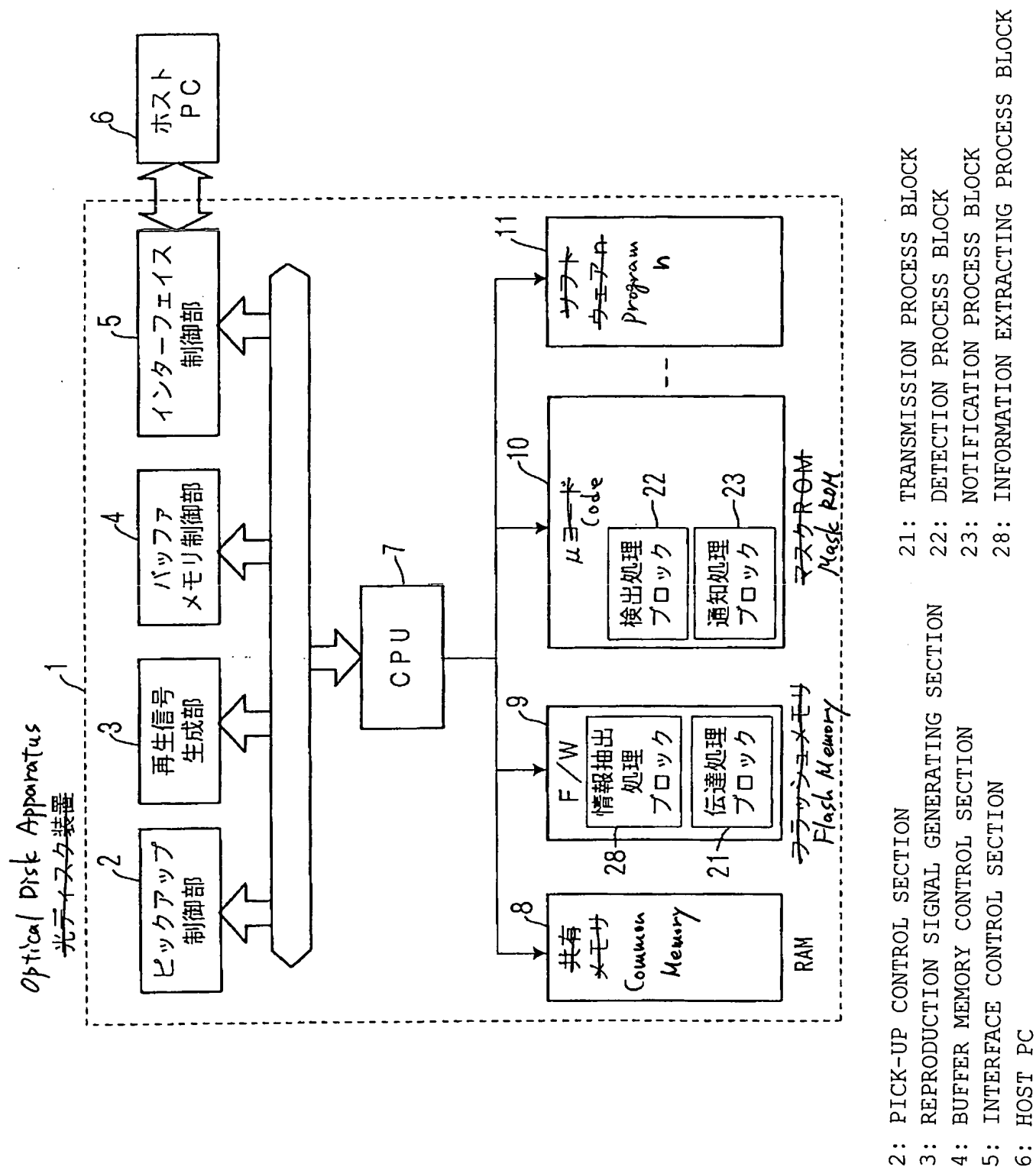
End Section:

- The disk controller issues a command (S39) to the host, which includes an Overhead and a READ(10) command.
- The disk controller performs final processing (S39) and issues a command (S38) to the host, which includes an Overhead and a READ(10) command.

S33: ANALYZE COMMAND
S34: DETECT DEFECTIVE BLOCK
S35: SEEK PROCESS
S36: ARD COMMAND
S37: BUFFER ALTERNATIVE BLOCK
S38: TRANSFER
S39: TERMINATING PROCESS

S33: ANALYZE COMMAND
S34: DETECT DEFECTIVE BLOCK
S35: SEEK PROCESS
S36: ARD COMMAND
S37a: BUFFER ALTERNATIVE BLOCK
S37b: BUFFER ALTERNATIVE BLOCK
S38: TRANSFER
S39: TERMINATING PROCESS

【図8】 FIG. 8



【図9】

FIG. 9A

Defective Block (a)

Alternative Block

MDT	DTB	Status 1	代替ブロック PBN	Status 2	代替ブロック PBN
0	0	0	0 05 A0	x	x xx xx
		1	0 06 75	x	x xx xx
		0/1	昇順値 ↓	x	x xx xx
		0	0 0F 75	x	x xx xx
		-2	0 00 00	x	0 04 00
		2	0 00 00	x	0 04 01
		2	0 00 00	x	0 04 02
		2	0 00 00	x	昇順値 ↓
		2	0 00 00	x	0 04 ff
		3	x xx xx	x	0 00 23
		3	x xx xx	x	任意の順値 ↓
		3	x xx xx	x	0 02 05
	1	1	0 1F 75	x	x xx xx
		0/1	昇順値 ↓	x	x xx xx
		:	:	:	:
		2	0 00 00	x	> 0 04 FF
		2	0 00 00	x	昇順値 ↓
		:	:	:	:
	2	0/1	etc		
		:	:	:	:
		2	0 00 00	x	etc
		:	:	:	:
		3	x xx xx	x	x xx xx
		:	:	:	:

FIG. 9B

00 00 05 A0	xx xx xx xx
00 10 06 75	xx xx xx xx
昇順値 ↓	xx xx xx xx
00 00 0F 75	xx xx xx xx
01 10 1F 75	xx xx xx xx
昇順値 ↓	xx xx xx xx
:	:
:	:
:	:

Value in
Ascending OrderValue in
Ascending OrderValue in
Ascending Order

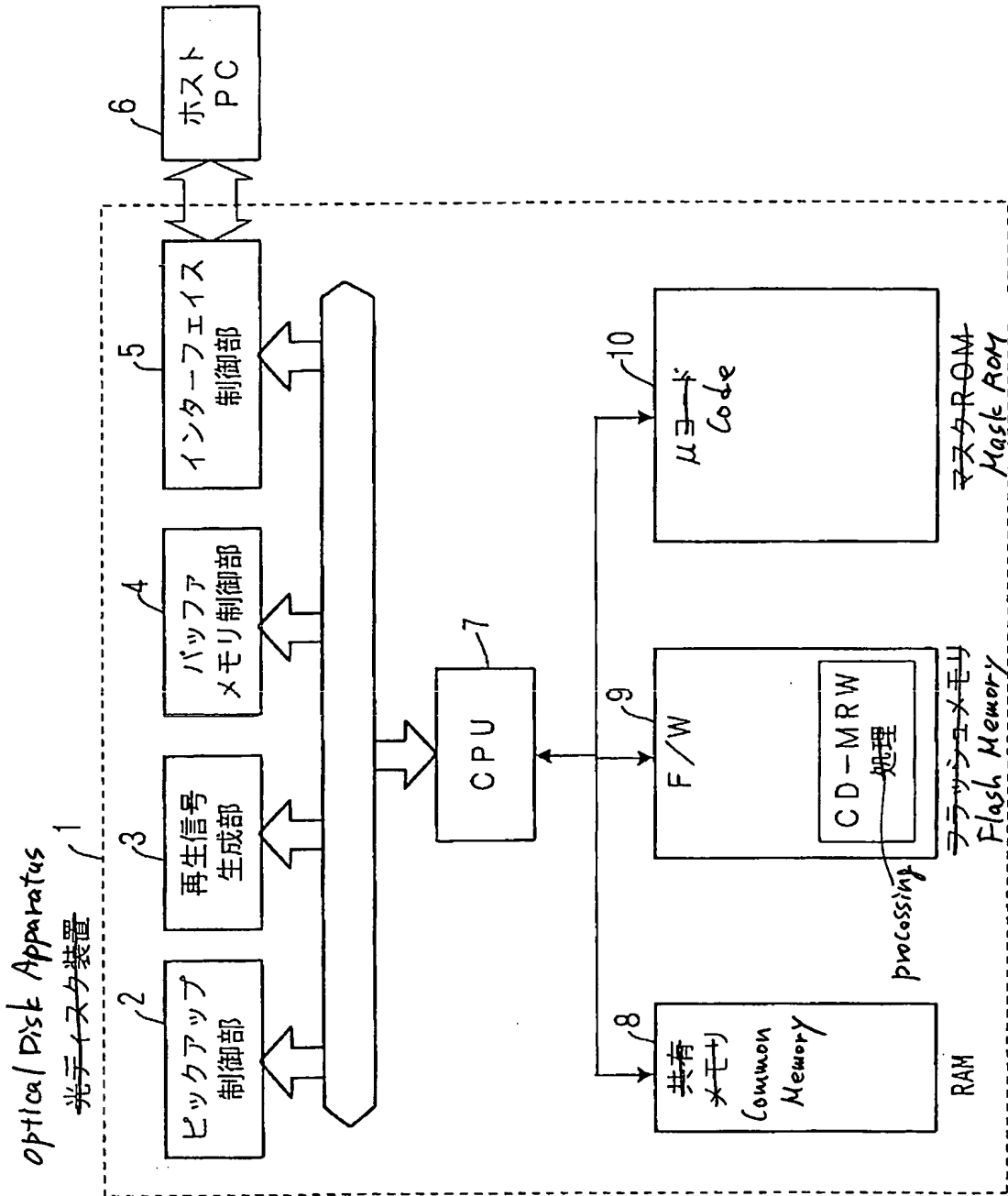
Value in Ascending Order

Arbitrary Order

Value in Ascending Order

Value in Ascending Order

~~図10~~ FIG. 10



- 2: PICK-UP CONTROL SECTION
- 3: REPRODUCTION SIGNAL GENERATING SECTION
- 4: BUFFER MEMORY CONTROL SECTION
- 5: INTERFACE CONTROL SECTION
- 6: HOST PC